What is claimed is:

1. A silicon on insulator (SOI) device substrate comprising a silicon carbide layer having formed thereon a dielectric layer.

2. The SOI substrate claimed in claim 1, wherein the dielectric layer is silicon oxide.

3. The SOI substrate claimed in claim 1, further comprising a layer of a semiconductor material formed on the dielectric layer.

4. The SOI substrate claimed in claim 1, wherein the semiconductor material is silicon.

5. The SOI substrate claimed in claim 1, wherein the semiconductor material is silicon germanium having a composition $Si_{1-x}Ge_x$, where x is in the range of 0.1 to 0.3.

6. The SOI substrate claimed in claim 1, wherein the silicon carbide layer is formed on a silicon oxide layer of a silicon wafer.

7. A silicon on insulator (SOI) device comprising:

a SOI substrate comprising a silicon carbide layer having a dielectric layer formed thereon; and

at least one metal oxide semiconductor field effect transistor (MOSFET) formed on the dielectric layer.

8. The SOI device claimed in claim 7, wherein the MOSFET comprises a silicon FinFET body

9. The SOI device claimed in claim 7, wherein the MOSFET comprises a silicon germanium FinFET body having a strained silicon layer grown on at least a channel region thereof.

10. The SOI device claimed in claim 9, wherein the silicon germanium has a composition $Si_{1-x}Ge_x$, where x is in the range of 0.1 to 0.3.

11. The SOI device claimed in claim 7, wherein the dielectric layer is silicon oxide.

12. The SOI device claimed in claim 7, wherein the SOI substrate further comprises a silicon layer formed on the dielectric layer, and

wherein the MOSFET is formed in an active region defined by shallow trench isolations extending through the silicon layer to the dielectric layer.

13. The SOI device claimed in claim 7, wherein the SOI substrate further comprises a silicon germanium layer formed on the dielectric layer, and

wherein the MOSFET is formed in an active region defined by shallow trench isolations extending through the silicon germanium layer to the dielectric layer.

14. A method of forming a silicon on insulator (SOI) device substrate, comprising:

forming a first dielectric layer on a silicon wafer;

forming a layer of silicon carbide over the first dielectric layer; and

forming a second dielectric layer on the silicon carbide layer.

15. The method claimed in claim 14, wherein forming the second dielectric layer on the silicon carbide layer comprises bonding the second dielectric layer to the silicon carbide layer.

16. The method claimed in claim 15, wherein the second dielectric layer is a silicon oxide layer formed on the surface of a semiconductor layer.

17. The method claimed in claim 16, wherein the semiconductor layer is a silicon layer.

18. The method claimed in claim 16, wherein the semiconductor layer is a silicon germanium layer.

19. The method claimed in claim 18, wherein the silicon germanium layer has a composition $Si_{1-x}Ge_x$, where x is in the range of 0.1 to 0.3.

20. The method claimed in claim 16, wherein the semiconductor layer comprises a hydrogen implanted region, and

wherein said bonding comprises placing the second dielectric layer and the silicon carbide layer in contact in a high temperature environment, whereupon the semiconductor layer is fractured in the hydrogen implanted region.

21. A method for forming a silicon on insulator (SOI) device, comprising:

providing an SOI substrate comprising a silicon carbide layer, a dielectric layer formed on the silicon carbide layer, and a layer of a semiconductor material formed on the dielectric layer;

patterning a FinFET body from the semiconductor material, the FinFET body comprising source and drain regions joined by a channel region;

forming a gate insulator around at least the channel region; and

forming a gate around the channel region, the gate being separated from the channel region by the gate insulator.

22. The method claimed in claim 21, wherein the semiconductor material is silicon.

23. The method claimed in claim 21, wherein the semiconductor material is silicon germanium having a composition $Si_{1-x}Ge_x$, where x is in the range of 0.1 to 0.3.

24. The method claimed in claim 23, wherein a layer of strained silicon is grown on the FinFET body prior to forming the gate insulator.

25. The method claimed in claim 21, wherein providing the SOI substrate comprises:

forming an insulating layer on a silicon wafer;

forming a layer of silicon carbide over the insulating layer; and

bonding said dielectric layer to the silicon carbide layer.

26. The method claimed in claim 21, wherein the silicon carbide layer of the SOI substrate is formed on a silicon oxide layer of a silicon wafer.

27. A method for forming a silicon on insulator (SOI) device, comprising:

providing an SOI substrate comprising a silicon carbide layer, a dielectric layer formed on the silicon carbide layer, and a layer of a semiconductor material formed on the dielectric layer;

forming shallow trench isolations that extend through the semiconductor material to the dielectric layer and define an active region of the substrate; and

forming a MOSFET in the active region.

28. The method claimed in claim 27, wherein the semiconductor material is silicon.

29. The method claimed in claim 27, wherein the semiconductor material is silicon germanium having a composition $Si_{1-x}Ge_x$, where x is in the range of 0.1 to 0.3.

30. The method claimed in claim 29, further comprising growing strained silicon on silicon germanium in the active region.

31. The method claimed in claim 27, wherein providing the SOI substrate comprises:

forming an insulating layer on a silicon wafer;

forming a layer of silicon carbide over the insulating layer; and

bonding said dielectric layer to the silicon carbide layer.

32. The method claimed in claim 27, wherein the silicon carbide layer of the SOI substrate is formed on a silicon oxide layer of a silicon wafer.